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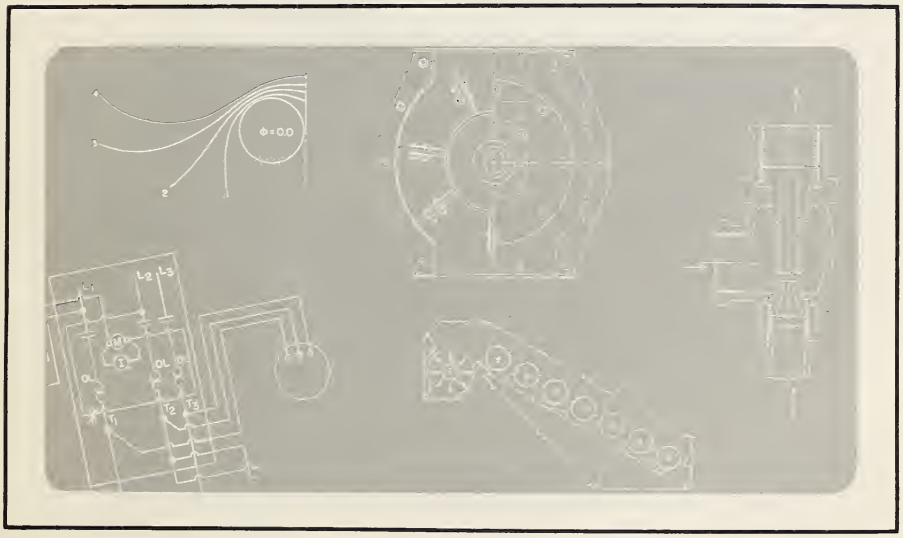
A Portable Self-Contained Data Acquisition and Retrieval System



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A Portable Self-Contained Data Acquisition and Retrieval System

By R. A. Stermer,[1] T. H. Camp,[2] and L. R. Smith[3]

ABSTRACT

Detailed schematics and procedures are given for constructing a battery-powered solid-state system for periodically taking such measurements as the temperature of plant products and animals in unattended remote locations. The small low-power acquisition module is directly wired to the sensors used and has a self-contained memory, eliminating the need for "hard wiring" or radiotelemetry to transmit data to an auxiliary storage device. The retrieval unit, which is connected to the acquisition module by cable through an integrated-circuit connecter, records data from any number of acquisition modules on cassette tape in a format suitable for computer processing. Performance data for a particular application are given. Index terms: data acquisition module, data processing, data retrieval and storage unit, solid-state electronics.

INTRODUCTION

There is frequent need in research and in the commercial transport of agricultural commodities or live animals to monitor environmental or product conditions on a periodic basis. If, for example, the temperature of such perishable commodities as fresh fruits and vegetables exceeds tolerable limits by a few degrees, serious damage can occur. In many research applications it is essential to monitor the product or animal in its natural environment. For example, monitoring the temperature of feeder calves during transportation from the producer to the destination feedlot could alert personnel there to be prepared to treat those calves having clinical signs (high body temperature) of an illness such as shipping fever (unpublished data).

Many devices have been developed for monitoring measurements such as temperature and relative humidity, but most of these require either the use of "hard wiring" or radiotelemetry. Temperature recorders, such as the Grant magnetic tape temperature recorder, are moderately compact and portable but require remote temperature sensors to be "hard wired" to them. Though such an arrangement is satisfactory for monitoring the environment in a transport vehicle, it becomes difficult to place the sensors in the product or product container because lead wires interfere with loading and unloading and are highly subject to damage. Such a system obviously cannot be used with free-ranging animals. Radiotelemetry using small transmitters (Stermer et al. 1980) eliminates the problem of "hard wiring," since the sensor can be a part of the transmitter, but this system has such limitations

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as limited distance between transmitter and receiver, number of radio channels available, and noise caused by radio interference.

The system described herein avoids these problems through direct-wiring of the sensor used to a small, low-power electronic module that uses solid-state memory devices as the data-storage media. This particular system was designed to be mounted on a halter for monitoring the body temperature of cattle. Simple modifications, such as changing the transducer and input amplifier, would allow the unit to be used to monitor other measurements, such as relative humidity.

DESIGN CONSIDERATIONS

The principal criteria used in designing the data acquisition system were to have (1) a minimal power requirement for the module, i.e., operation from a small battery for at least 20 days; (2) sampling periods of 1 h, 0.125 h, and about 3 s, the latter period for testing; (3) a memory capacity of at least 256 8-bit words; and (4) a rugged metal case not exceeding 2.5 by 5.0 by 10.0 cm in size for containing the module. The clock was to be accurate to within 1 min every 24 h. Also needed was a suitable temperature sensor and associated electronic circuitry having a resolution and accuracy of $\pm 0.1°$ C.

In addition to the data acquisition module, a system for orderly retrieval and mass storage of the data was needed. The design criteria for this unit were to (1) be capable of retrieving data from a number of data acquisition modules in an orderly manner, (2) be battery operated for use in remote locations, (3) be self-contained and portable, and (4) be capable of formatting in a computer-readable form. It was desirable to minimize the data-storage requirements of the data acquisition module but also to preserve the time and identity of data retrieved. Therefore, it was necessary for the retrieval unit to have provisions for semiautomatic recording of the time and identification (ID) number of the data acquisition module (corresponding to a particular animal number). It was still necessary for the user to manually record the time when the unit was started so that the time could be entered into the data retrieval unit when the data were transferred to magnetic tape.

Two of the prime requirements mentioned above were low power and small physical size. The ideal would have been a uniquely designed integrated circuit for each of the modules. However, an investigation of this process showed that the development cost would have been excessive ($5,000 to $10,000). Therefore, we decided to use a compact arrangement of discrete components and commercially available integrated circuits (I.C.'s) mounted on printed circuit (p.c.) boards.

Technology involving complementary metal-oxide semiconductors (CMOS) possesses a number of advantages over other forms such as diode- and transistor-transistor logic (TTL). Recent technological advances have allowed construction of CMOS circuits that have extremely low power requirements (single supplies down to 1.5 V), high noise immunity, high density, and high reliability in harsh environments (Fisher and Young 1979, Calebotta 1978). CMOS memory units can now be constructed that do not require extensive refresh logic and that are tolerant of wide fluctuations in supply voltage. One of the major applications, of course, has been in microprocessors and calculators. Other uses include timekeeping (a function needed in the data acquisition system), telecommunications, and medical electronics.

CIRCUIT DESCRIPTIONS

The values of all resistors shown on the schematics in this report are in ohms. All resistors used in the data acquisition module are 1/10 W, carbon film, with 5% tolerance. All resistors in the data retrieval and recorder unit are 1/4 W, carbon film, with 5% tolerance. Specifications are also listed in appendices I–K. The values of all capacitors are in microfarads (μF) unless otherwise indicated on the schematics and in these appendices. Other specifications, such as type, voltage rating, and tolerance, are also listed in appendices I–K.

Data Acquisition Module

A block diagram of the data acquisition module is shown in figure 1, and a schematic of the module is shown in figure 2.

A thermistor probe, located in the variable leg of a d.c. Wheatstone bridge, is used as the temperature sensor. We use a Yellow Spring Instruments 17091 thermistor probe that has a

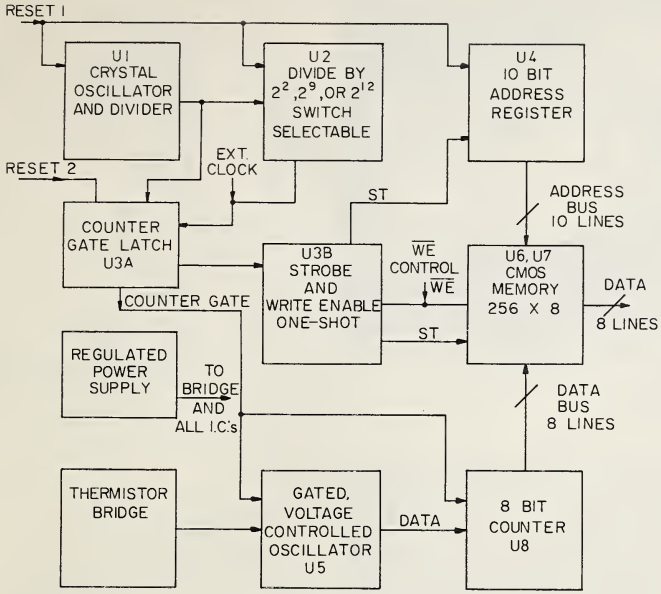


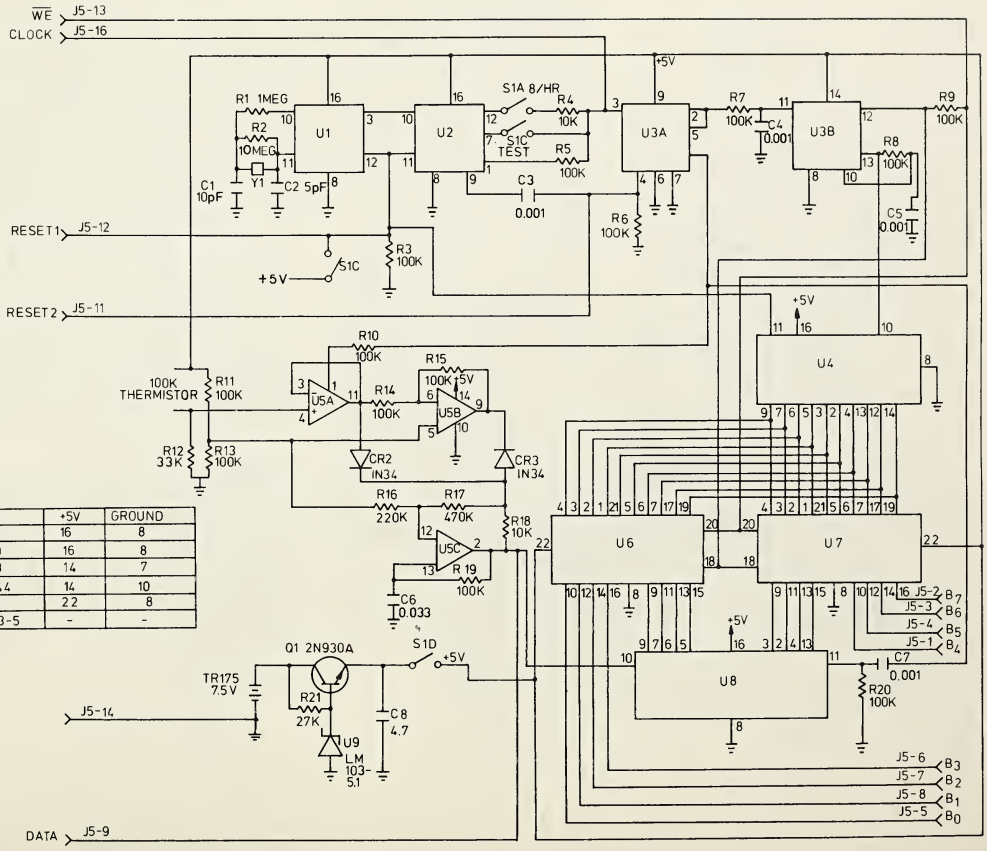
FIGURE 1.—Block diagram of data acquisition module.

nominal resistance of 100 kilohms at 25° C and an interchangeability factor of 0.2° C. For monitoring the temperature of cattle, the thermistor-probe is inserted in the ear near the tympanic membrane. A pour-in-place foam elastomer is used to hold the probe in place as well as insulate it from ambient air.

Precision, interchangeable thermistors, which are generally of the wafer or "chip" type, have the advantage of allowing the use of one calibration curve (resistance vs. temperature) for all thermistors. However, they are subject to drift, apparently attributable to peculiar a.c. impedance characteristics when a.c. accelerating potentials are applied to them. We have avoided this problem by using the d.c. bridge. We have determined that glass-bead thermistors are not seriously affected by alternating current and thus would eliminate the need for the Wheatstone bridge, since the thermistor could be placed in the feedback loop of the oscillator. This arrangement would require calibration of each module with a particular thermistor.

Since the Wheatstone bridge and oscillator U5 are highly sensitive to changes in supply voltage, a d.c. voltage regulator circuit (lower left in figure 2) having a low parasitic current (35μA) was designed. A single 7.5-V battery, Mallory TR 175 or equivalent, supplies power to the module. Tests have shown that this battery will last about 5 weeks when the sampling rate of the data acquisition module is one sample per hour. The key to the operation of the regulated power supply is voltage reference diode U9 in the base circuit of Q1 (fig. 2). A performance test of the voltage regulator (table 1) showed that the regulation was very good over the useful range of battery voltage (5.5 to 7.4 V). Output voltage varied by only 0.3% (0.012 V), resulting in an equivalent temperature change of 0.025° C.

A stable time base is generated by crystal oscillator-counter U1. The frequency of crystal



REF DES	TYPE	+5V	GROUND
U1	4060	16	8
U2, U4, U8	4040	16	8
U3	4013	14	7
U5	L-144	14	10
U6, U7	6551	22	8
U9	LM-103-5	-	-

FIGURE 2.—Schematic of data acquisition module. MEG=megohm; K=kilohm.

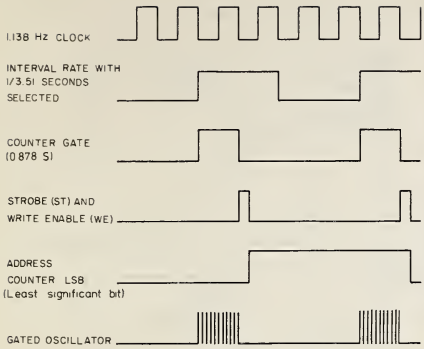


FIGURE 3.—Timing diagram of data acquisition module in autonomous mode.

FIGURE 5.—View of assembled data acquisition module.

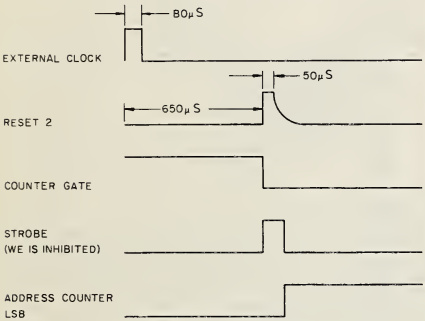


FIGURE 4.—Timing diagram of data acquisition module in manual mode.

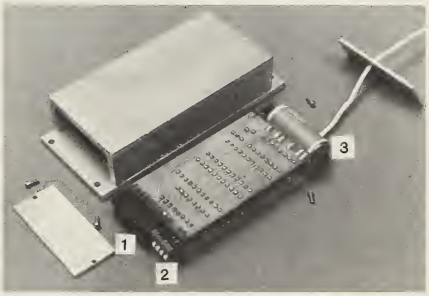


FIGURE 6.—View showing arrangement of electronic components and printed-circuit boards in data acquisition module. 1, Connecter J5. 2, Switch S1. 3, Battery.

Table 1.—Summary of test results of voltage regulator and oscillator frequency stability

Battery voltage	Voltage out	Oscillator frequency[1]
7.4	4.5174	164.1
6.4	4.5145	163.9
5.5	4.5055	163.6

[1]With fixed resistance in lieu of thermistor.

Y1 (fig. 2) is 18.641 kHz, since this value is divisible by 3,600 to provide a 1-h gate without additional decoding. Two binary switches (S1a and S1b), in conjunction with counter U2, allow intervals of 3.5 s, 7.5 min, and 1 h to be selected. The selected interval-rate clock pulse (fig. 3) is used to trigger counter-gate latch U3a. The $\overline{\text{STROBE}}$ ($\overline{\text{ST}}$), and $\overline{\text{WRITE ENABLE}}$ ($\overline{\text{WE}}$) one-shots are then triggered by the trailing edge of the counter gate. One-half of a dual, type D flip-flop is connected as a one-shot to decrease the number of I.C.'s required. The trailing edge of $\overline{\text{ST}}$ increments address register U4. The number of

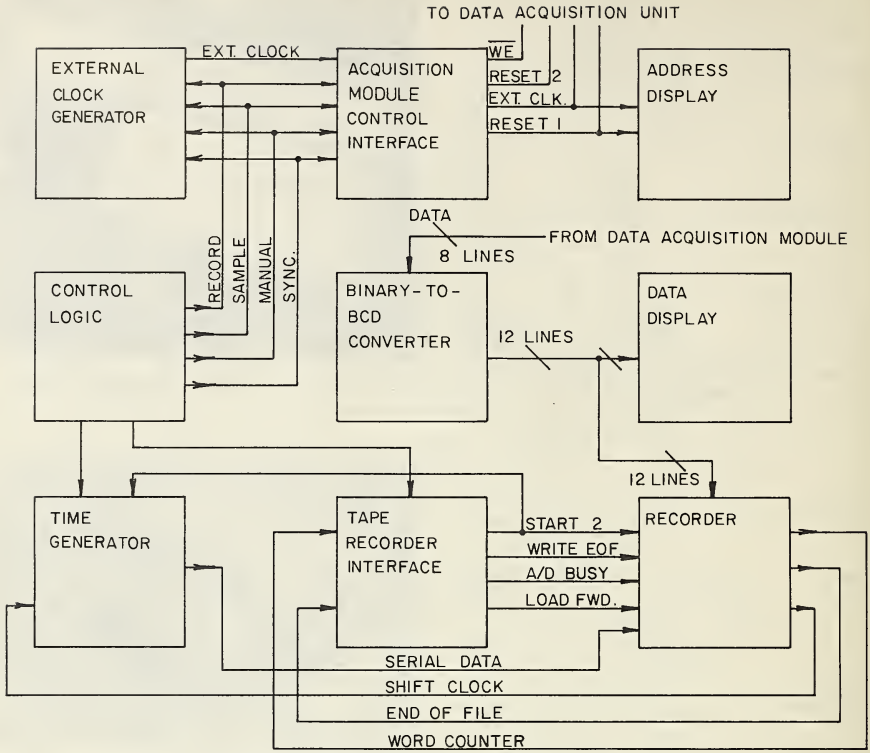


FIGURE 7.—Block diagram of data retrieval and recorder unit.

pulses generated by gated oscillator U5 is counted by 8-bit counter U8. The data word from U8 is stored at the address location contained in address register U4 on the occurrence of $\overline{ST}$ and $\overline{WE}$. $\overline{WE}$ is delayed until the data and address buses are stable. The count of pulses per sampling period is proportional to temperature and is stored in memory as an 8-bit word. The memory, U6 and U7, has a capacity of 256 words, which could be expanded to 512 words.

RESET 1 (figs.1 and 2) resets memory address register U4 and the divider network, U1 and U2. This signal can be generated either internally by a switch in the data acquisition module or externally by the data retrieval and recorder unit. RESET 2 (figs. 1 and 2), generated in the data retrieval and recorder unit, shortens the sample command gate to allow rapid advance of memory address register U4 during MANUAL FAST examination of stored data. All other signals shown entering or leaving the data acquisition module connect to the retrieval unit.

The timing diagram for the data acquisition module, when operated in the MANUAL mode, is shown in figure 4. This mode allows the contents of memory to be displayed and examined. The address counter is stepped each time the "step" switch is depressed. $\overline{WE}$ is inhibited by the data retrieval and recorder unit when in the manual mode.

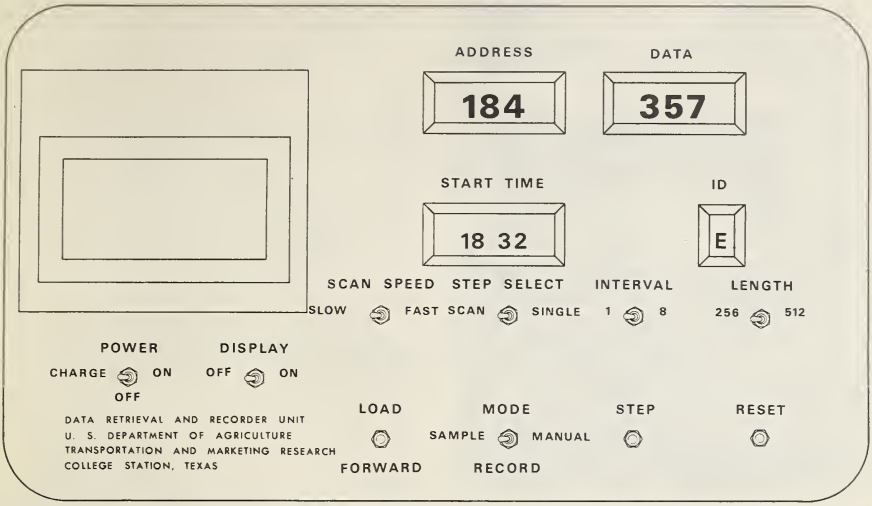


FIGURE 8.—Control panel of data retrieval and recorder unit.

Using the system to monitor the body temperature of cattle, a range of 33° to 45° C (91° to 133° F) is adequate. This range provides a resolution of 0.047° C, limited by the 8-bit word size. If users are interested in a wider range, they can sacrifice resolution or increase the word size of memory.

An assembled data acquisition module is shown in figure 5, and the module with the case removed is shown in figure 6. (Note the compact arrangement of the p.c. boards and components to conserve space.) A 16-pin I.C. socket (J5) is used to connect the data acquisition module to the data retrieval and recorder unit when data are transferred to a cassette tape. A quad single-pole single-throw, dual-inline-pin (DIP) switch is used to turn the data acquisition module on or off, reset the memory address register, and select the time interval between data words. The data acquisition module is housed in a rugged aluminum case 45 mm wide, 90 mm long, and 20 mm high. A list of parts for the module is shown in appendix I.

Data Retrieval and Recorder Unit

This unit consists of nine subassemblies (fig. 7) and an operator's control panel (fig. 8). The unit provides the control circuitry to (1) retrieve the data from the memories of the data acquisition modules in an orderly manner, (2) convert the data from binary to binary coded decimal (BCD), (3) generate the time that data are taken, (4) generate the ID number of the data acquisition module, and (5) record the data on magnetic tape in a form suitable for computer processing.

The mechanical layout of the data retrieval and recorder unit (fig. 9) is as follows. The external-clock generator, acquisition module interface, control logic, time generator, and tape recorder interface are on one p.c. board (logic board). The placement of I.C.'s, transistors, and cable tie points is shown in figure 10. The binary-to-BCD converter is on another p.c. board. Locations of

(*Continued on page 10.*)

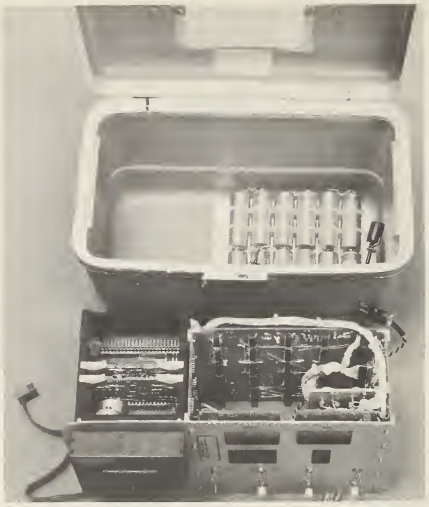


FIGURE 9.—Interior view of data retrieval and recorder unit.

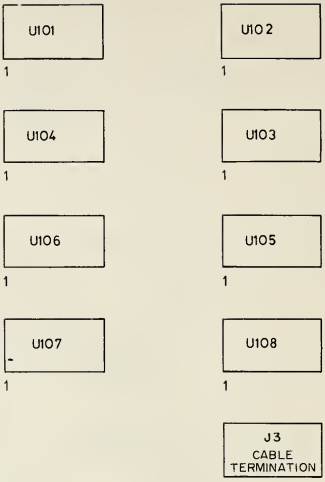


FIGURE 11.—Placement diagram of binary-to-BCD board components.

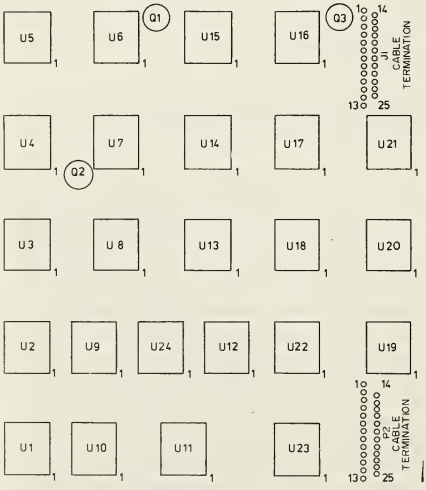


FIGURE 10.—Placement diagram of logic-board components.

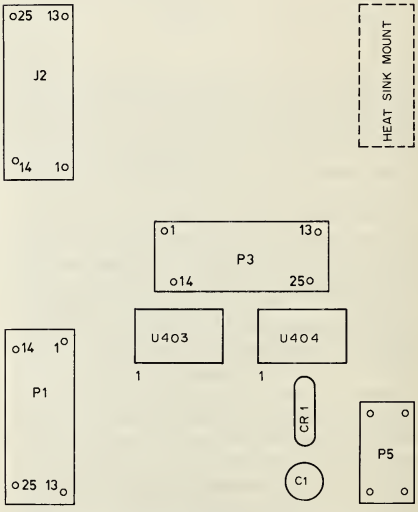


FIGURE 12.—Placement diagram of connecter-board components.

Table 2.—Component labeling system

Subassembly	Component or connecter No.	Examples[1]
Data acquisition module	Units, tens	U1, R14, C8.
	J5	J5-2.
Logic board, data retrieval and recorder unit.	Units, tens	U24A, R25, C6.
	P1, J2	P1-20, J2-16.
Power supply, connecter board	J1, P2, J3, P5, J6	J1-7, P2-4, J3-10, P5-6, J6-3.
Binary-to-BCD converter, data retrieval and recorder unit.	One hundreds	U106D, R108.
	P3	P3-3, P3-22.
Tape cassette recorder	P6	P6-W, P6-L.
Tape cassette recorder interface	[2]	[2].
Address display, data retrieval and recorder unit.	Two hundreds	U202, Q206.
Data display, data retrieval and recorder unit.	Three hundreds	U302, R301.

[1]Explanation: the number, i.e. 2, following the dash in J5-2 refers to pin 2 of J5.
[2]See logic board for units used and examples.

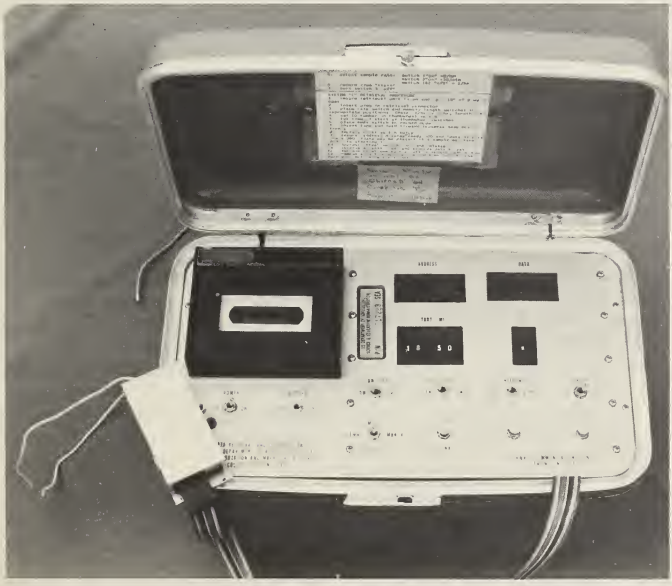


FIGURE 13.—View showing control panel of data retrieval and recorder unit.

I.C.'s are shown in figure 11. A third p.c. board (fig. 12) contains the power supply and serves as an interconnection point between the front panel and each of the other p.c. boards. All operator controls are on the front cover panel (fig. 13). The battery pack is in the bottom of a fiberglass luggage case 230 mm wide, 380 mm long, and 205 mm high.

A component labeling system (table 2) was adopted in this publication to permit the reader to more easily identify components of a particular subassembly.

Connections for power supply and subassemblies

Since the system is to be used in remote locations where 120-V a.c. power is not available, the data retrieval and recorder unit is also battery powered. A step-down transformer (T1) provides power to recharge a 16-V nicad battery pack. The charger and +5- and +12-V regulator circuits are shown in figure 14. Many of the signals entering and leaving the connecter board require "pull up" (to +12 V) or "pull down" (to ground) resistors.

Mode control logic

This subassembly (fig. 15) determines the operating mode of the data retrieval and recorder unit and is the most important of all the subassemblies because it performs the "housekeeping" functions of other subassemblies. The operator may select the following modes with MODE switch S6:

1. MANUAL—In this mode, the contents of memory are displayed. The address counter is advanced each time MEMORY STEP switch S4 (fig. 16) is depressed. If SCAN control switch S3 (fig. 16) is in the SCAN position, the address counter advances automatically.

2. SAMPLE—In this mode, the data are sampled and stored in memory address zero each time the MEMORY STEP switch is depressed.

3. RECORD—In this mode, the address counter is reset to zero and then automatically advanced sequentially from memory address zero to memory address 256 or 512. Partial reading of the memory is not permitted; all 256, or 512 for expanded memory, positions will be read after MEMORY STEP switch S4 is depressed once. After this switch has been depressed once, the MEMORY STEP, RESET, and SCAN SPEED controls become inoperative.

This subassembly contains two other controls, RESET switch S5 and SAMPLE INTERVAL switch S7 (fig. 15). In the SAMPLE and MANUAL modes, the RESET switch resets the address counter to zero each time it is depressed and released. In the RECORD mode, the recording cycle is reset, but the RESET switch is then inoperative until the contents from all 256 or 512 memory addresses have been recorded. SAMPLE INTERVAL switch S7 allows the operator to select 0.125 h or 1 h, whichever has been used when collecting the data on a particular data acquisition module.

This subassembly also generates a DATA SELECT flag, Q output of U14A, which controls the output of data to the recorder data bus.

External clock generator

This subassembly (fig. 16) is the basic timing unit. I.C.'s U1C, U1D, and U5 provide two clock rates, about 1 and 20 Hz, selected by SCAN SPEED switch S2 in the MANUAL mode. In the SAMPLE and RECORD modes, this switch is inoperative. In the RECORD mode, scanning is performed at the SLOW or 1-Hz rate. This subassembly also contains SCAN CONTROL switch S3, which is operative only in the MANUAL mode. When S3 is in the SINGLE position, the address counter is advanced one count each time MEMORY STEP switch S4 (discussed above) is depressed and released. When S3 is in the SCAN position, the address counter is advanced at a rate determined by the setting of SCAN SPEED switch S2. MEMORY SIZE SELECT switch S1 is provided to allow for future expansion of memory from 256 to 512 locations.

This subassembly also generates the RECORDER ENABLE flag, output of U2E, which disables MEMORY STEP during recording and generates a RESET 1 to the data acquisition module when recording is done. RESET 1 also resets the memory address counter to zero.

Control interface to data acquisition module

This interface (fig. 17) makes use of basic timing pulses generated by the external clock gen-

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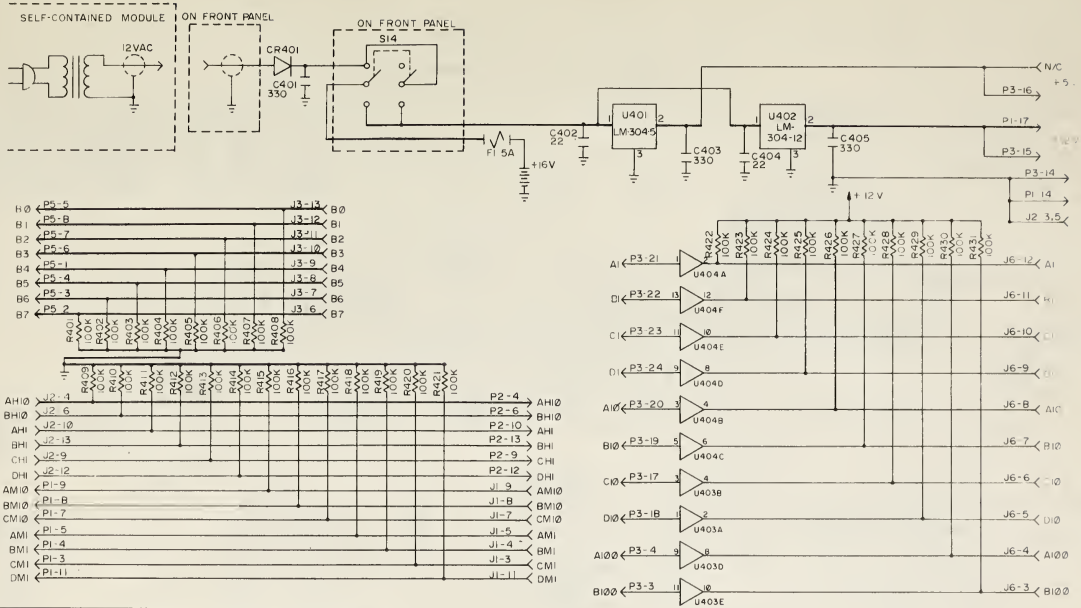
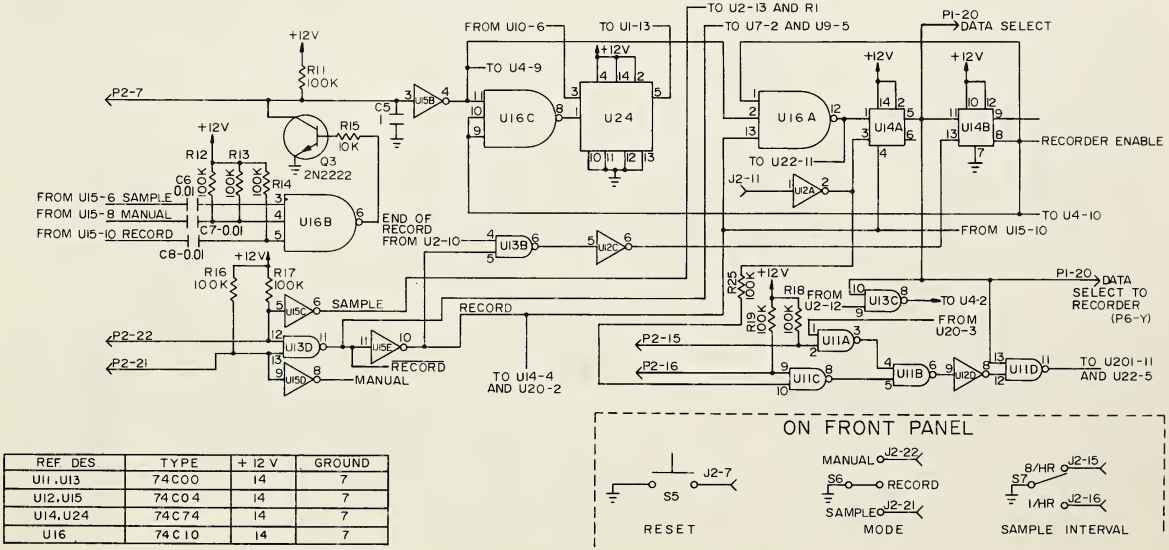


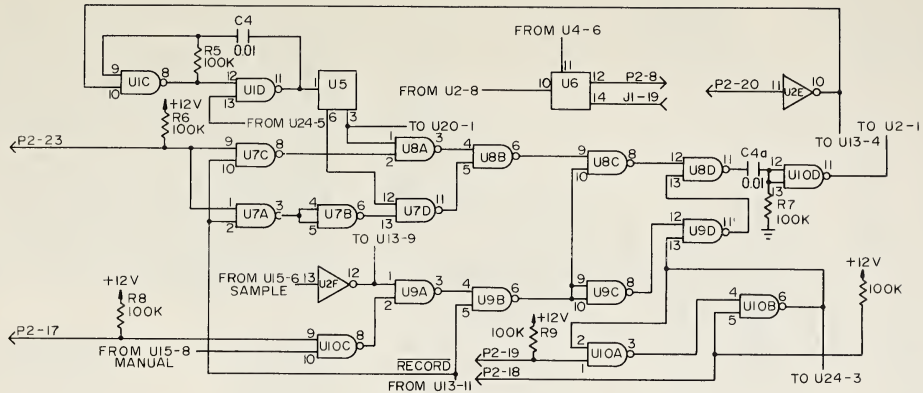
REF DES	TYPE	INPUT	OUTPUT	GROUND	Vcc
U401	LM-304-5	1	2	3	
U402	LM-304-12	1	2	3	
U403, U404	7205			7	14

FIGURE 14.—Schematic of power supply and connecter board. K=kilohm.



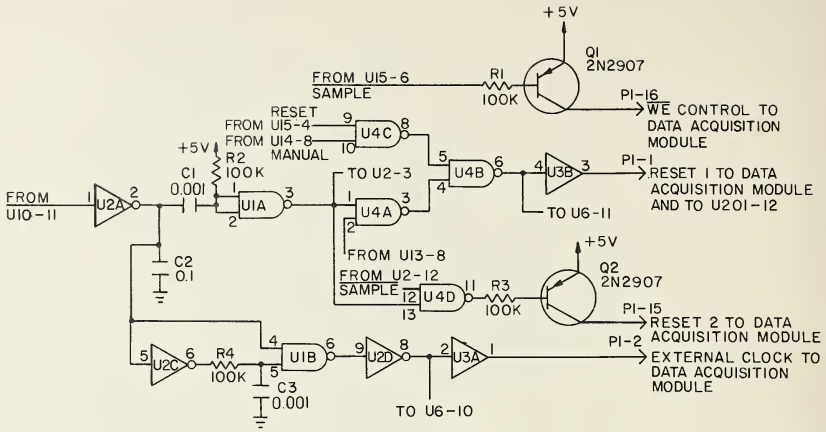
REF DES	TYPE	+ 12 V	GROUND
U11, U13	74C00	14	7
U12, U15	74C04	14	7
U14, U24	74C74	14	7
U16	74C10	14	7

FIGURE 15.—Schematic of mode control logic. K=kilohm.



REF DES	TYPE	+12V	GROUND
U1, U7, U8, U9, U10	74C00	14	7
U2	74C04	14	7
U5	4024	14	7
U6	4040	16	8

FIGURE 16.—Schematic of external clock generator. K=kilohm.



REF. DES.	TYPE	+12V	GROUND
U1,U4	74C00	14	7
U2	74C04	14	7
U3	74C902	14	7

FIGURE 17.—Schematic of control interface to data acquisition module. K=kilohm.

erator (fig. 16). These clock pulses are shaped to precise widths for timing the data acquisition module when data are transferred from memory to magnetic tape. Signals from the mode control unit (fig. 15) are used to provide further control of the data acquisition module.

Tape cassette recorder

The recorder used in this system is a Datel Intersil model ICT-WZ1B2B. It is an ultra-low-power (700 mW during writing), incremental, digital cassette recorder. It employs a Phillips cassette with a capacity of 3,200 files or sixty-four 8-bit characters per file and operates on 12 V d.c. An optional "formatter" board is used to format the data in a form suitable for computer processing (see appendix A). A Datel Intersil model LPR-16 cassette reader is interfaced via an RS 232 port to a Data General NOVA 3/12 minicomputer to permit rapid transfer of data to the computer memory for processing.

Several jumper connections must be made inside the Datel recorder. Since this system has been designed to accept eight words of data per file (see appendix A), a signal from the 8 WORD COUNTER must be returned to the tape recorder interface (fig. 18). This signal is obtained by connecting pad 12 on the formatter card of the Datel recorder to pin 8 of the card edge connecter, which in turn is connected to user edge connecter pin J (see appendix H). In this system, the female connecter is labeled J6, and the mother-board edge connecter of the recorder is labeled P6. Since all signals from the tape recorder interface are digital, an analog-to-digital converter is not required. However, if Datel model ICT-WZ1B2B recorder is used, the following jumper connections on the mother board are required: pins 1-12 of J4, analog-to-digital (A/D) converter jack, are

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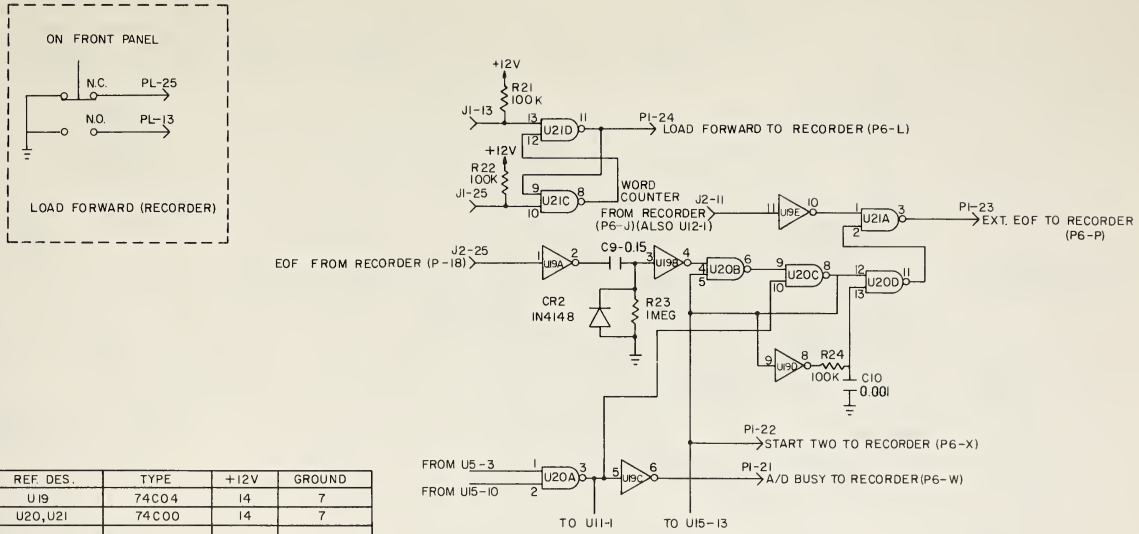
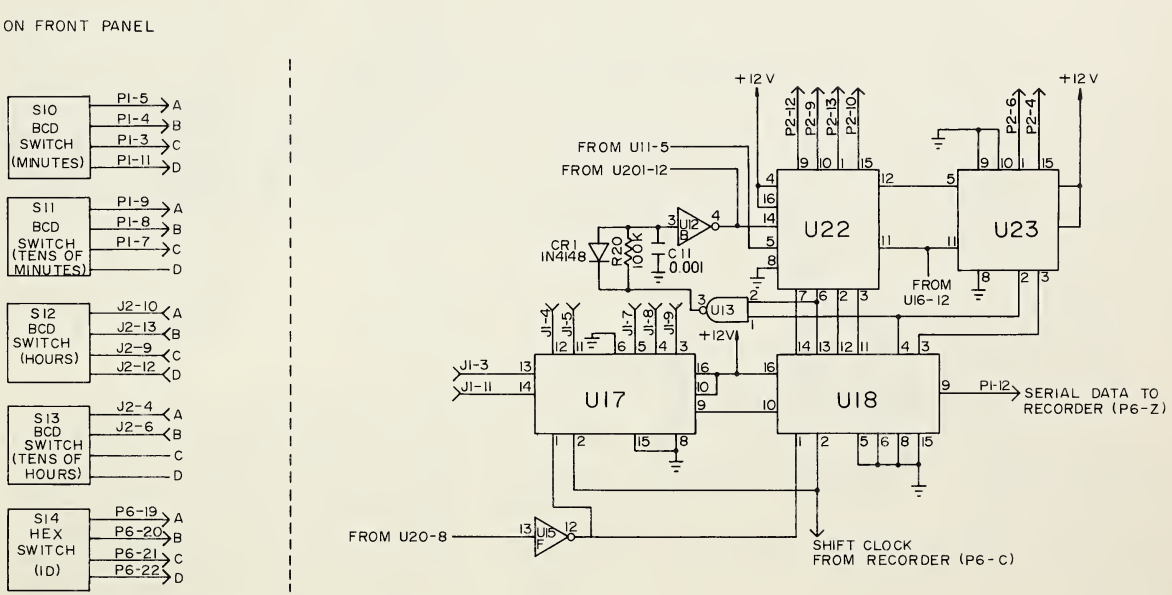


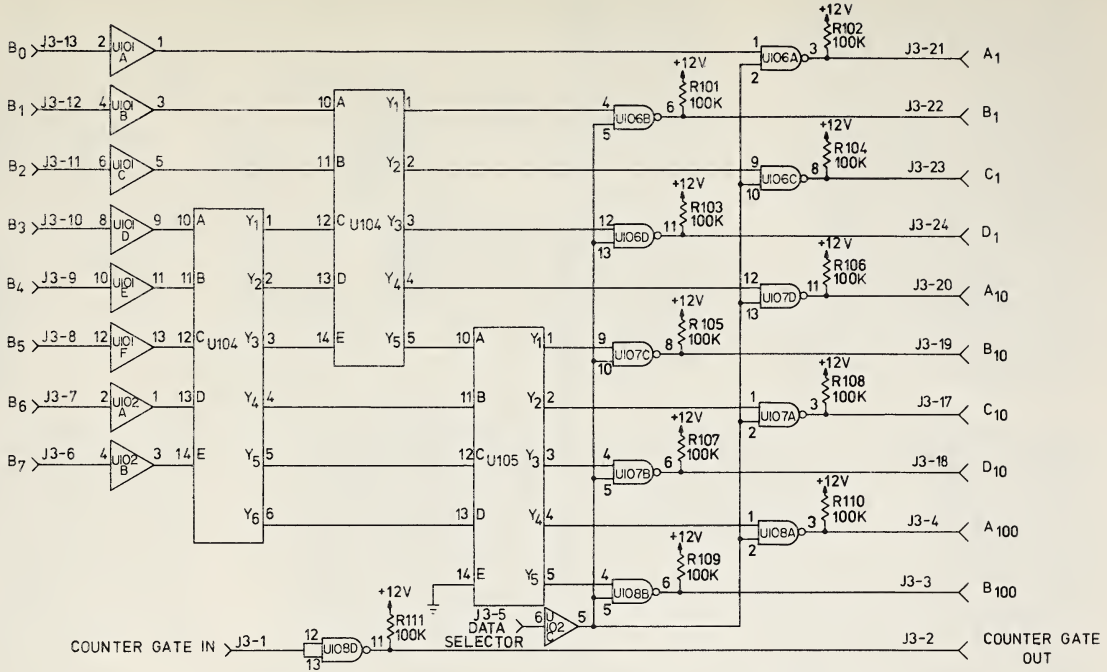
REF. DES.	TYPE	+12V	GROUND
U19	74C04	14	7
U20, U21	74C00	14	7

FIGURE 18.—Schematic of tape recorder interface. MEG=megohm; K=kilohm.



REF. DES.	TYPE	+12 V	GROUND
U15, U12	74C04	14	7
U13	74C00	14	7
U17, U18	74C165	16	8
U22, U23	74C192	16	8

FIGURE 19.—Schematic of time-generation and serial-data control. K=kilohm.



REF DES	TYPE	+5V	GROUND
U101, U102	74C902	14	7
U104, U105	74185A	16	8,15
U106, U107, U108	74LS26	14	7

FIGURE 20.—Schematic of binary-to-BCD code converter. K=kilohm.

connected to pins 1–12, respectively, of J5, multiplexer/sample-and-hold (MUX/S&H) card jack. The existing trace from pin 11 of J5 to pin 18 of P1 and pin 5 of J4 is cut at pin 11 of J5. Also, for the serial-data input, jumper pins 19–22 of J5 are connected to pins W–Z, respectively, of J3, formatter-card jack. If another recorder is used, the manufacturer's suggested diagram should be followed.

Tape recorder interface

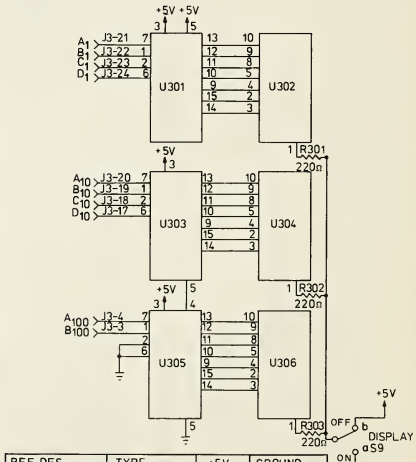
This subassembly (fig. 18) generates the controls for the recorder. The 1-s CLOCK and RECORD signals are AND-ed together to form an A/D BUSY signal. When this signal is low, parallel data (a frequency corresponding to a temperature plus a unit ID number) can be written onto tape. When the START 2 signal (output of U20C) is low, serial data ("Time" appearing as a trailer following each line per file of data) are written onto tape (appendix A). WORD COUNTER is a signal returned from the recorder to notify the tape recorder interface that eight words have been written and that an end-of-file (EOF) signal should be generated and sent to the recorder for recording. When the recorder has completed writing the EOF, it returns a signal to the tape recorder interface (input to U19A), which in turn allows START 2 to go low. One other convenience signal, LOAD FORWARD, is generated by U21C and U21D in conjunction with LOAD FORWARD switch S8. This signal allows the operator to advance tape past the clear leader and at any other place desired, such as spacing between data from different data acquisition modules.

Time-generation and serial-data control

This subassembly is not essential to the operation of the remainder of the system. However, it provides convenience for processing the data at a later time. The time-generation circuit (fig. 19) contains four thumb-wheel switches, S10–S13, that are used to dial in the time that a data acquisition module is started. Since the units and tens of minutes never change, they are simply loaded into shift register U17 and not incremented. Units of hours, however, are incremented after each word for the interval rate of 1 word per hour or after eight words for the interval of 8 words per hour by counters U22 and U23. These data are shifted out to the tape recorder when the A/D BUSY signal is low and are written as a trailer to the temperature data and ID number (see appendix A). The ID number of a particular data acquisition module is dialed into hexadecimal (HEX) switch S14 before the transfer of data to magnetic tape. These data are supplied to the tape recorder as serial data whenever START 2 is low and follow a space following the temperature data. The use of hexadecimals allows the inclusion of 16 unique ID numbers in a single character space in the formatted data (see appendix A).

Binary-to-BCD code converter

The temperature (frequency) data are stored in the memory of the data acquisition module as two 4-bit (hexadecimal) bytes (fig. 2). The two bytes are transferred to memory in parallel to form an 8-bit word, two hexadecimal digits. This conversion is rather awkward to accomplish, especially during calibration of the modules; therefore, a



REF DES	TYPE	+5V	GROUND
U301, U303, U305	74C48	14	7
U302, U304, U306	7740	-	-

FIGURE 21.—Schematic of data display.

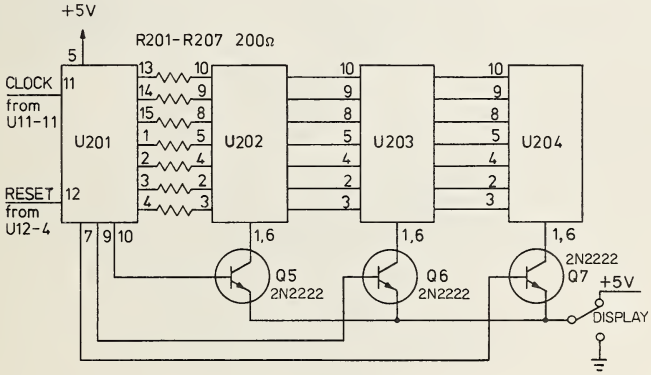
binary-to-BCD code converter (fig. 20) is used. The data are then displayed and recorded on magnetic tape in decimal form. This subassembly also contains logic level shifters (5- to 12-V d.c.) for those signals being transferred from the data acquisition module to the data retrieval and recorder unit.

Address and data displays

The data display (fig. 21) simply displays the BCD data for the operator's convenience during such operations as calibrating a data acquisition module or, when in the SAMPLE mode, determining if a module is obtaining the correct data.

The address display (fig. 22) displays the address of the memory location being observed. A counter (U201) counts the external clock pulses following a RESET so that the address displayed corresponds to the memory location being sampled in the data acquisition module. This logic is installed in lieu of having all the address lines come out of the data acquisition module, which would require additional wires and a connecter with more contacts and thus substantially increase the size of the module.

(*Continued on page 22.*)



REF. DES.	TYPE	+5V	GROUND	
U201	74C925	16	8	
U202	7740	—	—	
U203	7740	—	—	
U204	7740	—	—	

FIGURE 22.—Schematic of address display.

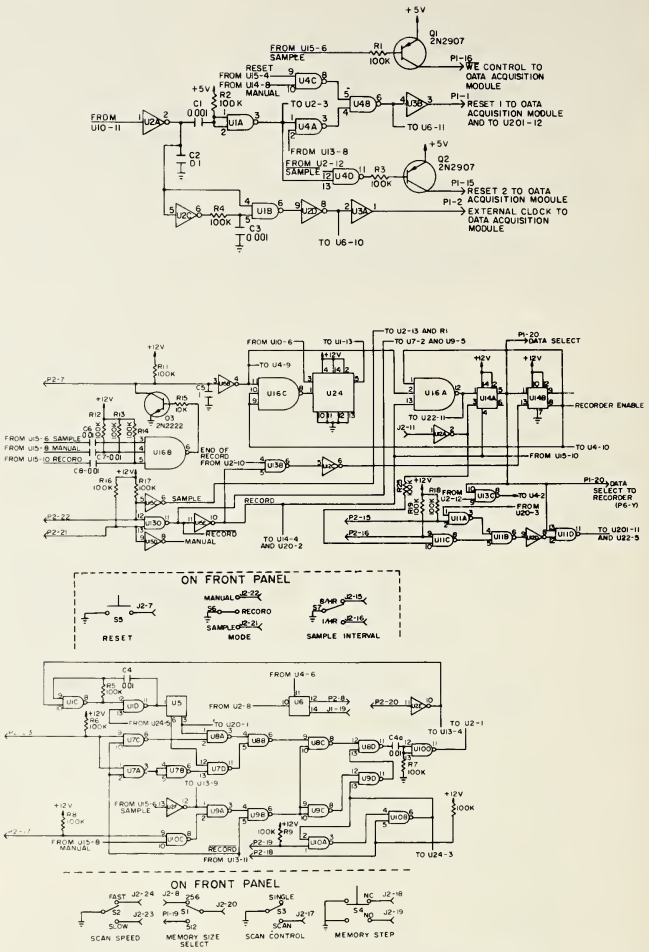
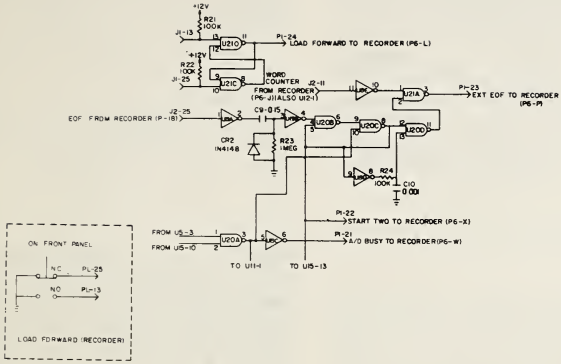
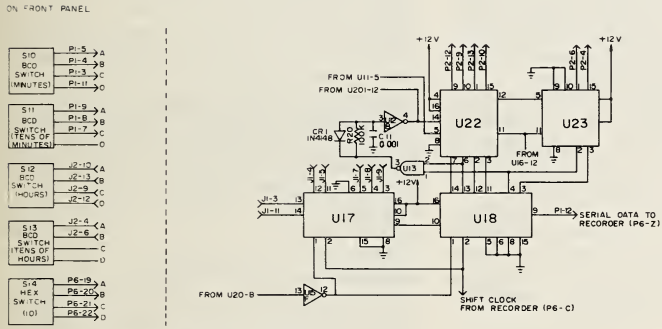


FIGURE 23.—Composite schematic of data retrieval





and recorder unit. MEG=megohm; K=kilohm.

DETAILED PROCEDURES FOR OPERATION OF DATA RETRIEVAL AND RECORDER UNIT

The following detailed operating procedures for this unit are presented for the reader who may be interested in more detail than is given above. We suggest that those interested in this section reproduce figures 15–19 and form a composite similar to the one in figure 23. Considerable interaction occurs among various subassemblies in each of the three modes. Therefore, the composite schematic will assist the reader in following the discussion without having to move from figure to figure.

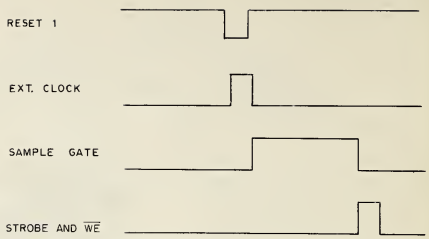


FIGURE 24.—Timing diagram for data retrieval and recorder unit in SAMPLE mode.

SAMPLE MODE

A timing diagram for the unit in the SAMPLE mode is shown in figure 24. When MODE switch S6 is moved to the MANUAL position, a synchronizing (SYNC) pulse is generated by the network involving U15B, which disables the external clock (U1C, U1D, and U5). The RECORD signal is low, which causes U14A to be set. The high signal at U14-8 enables U16C. The high SAMPLE signal on the base of Q1 creates a high Z (impedance) state. In this state, the collector is neither high nor low but rather appears as an open circuit, sometimes called tristate, to the $\overline{WE}$ control of the data acquisition module.

The low MANUAL signal at U10-10 disables MEMORY STEP switch S4, and the $\overline{SAMPLE}$ signal at U9-1 results in an enabling high at U9-4. This signal NAND-ed with the $\overline{RECORD}$ signal drives U9-6 low, disables U8C, and enables U9D. When MEMORY STEP switch S4 is depressed and released, the falling edge of the pulse at U9-11 causes a high signal on the pulse generator network (C4a, R7, and U10D). The trigger from U10-11 is inverted and shaped by U2A and U1A to create a RESET pulse at U4-1. Since U4-2 is high in the SAMPLE mode, the pulse is passed to the data acquisition module. This pulse resets the timing chain and address register. C2 causes a slight delay (about 100 μs) in the generation of an external clock pulse (fig. 24) by U2C and U1B. While the reset pulse holds the clock chain signal low, the external clock pulse sets the SAMPLE gate flip-flop signal high. When the clock pulse goes low, the $\overline{WE}$ signal also goes low and allows the data to be written in memory address zero. Since the address is monitored by the binary-to-BCD converter (fig. 20) and the DATA SELECT latch is held set, the data are displayed as a three-digit decimal number as soon as the write cycle is complete.

MANUAL MODE

A timing diagram for the unit in the MANUAL mode is shown in figure 25. As in the SAMPLE mode when MODE switch S6 is moved to MANUAL, a SYNC pulse is generated. DATA SELECT (Q output of U14A) is held set by the low RECORD signal. RECORDER ENABLE (U14-8) is held reset by the low signal at U12-6. The $\overline{RECORD}$ signal from U13-11 enables U9B and U7C, which enables the SCAN SPEED control and allows the selection of FAST or SLOW memory stepping. $\overline{MANUAL}$ enables SCAN CONTROL switch S3. If this switch is in the SINGLE position, a low signal is generated by U10C, which drives U9-3 high. This high signal NAND-ed with the $\overline{RECORD}$ signal drives U9-6 low, which disables the clock signal at U8-8 and enables the STEP SELECT flip-flop signal (U10A and U10B). If S3 is in the SCAN position, the low input at U10-9 drives U10-8 high. This signal is NAND-ed with the $\overline{SAMPLE}$ signal (U9A). The low signal at U9-4 drives U9-6 high, which disables the STEP flip-flop output (U9-11) and enables the clock signal to the external clock generator (U10-11).

The clock rate at U8-6 is determined by the setting of SCAN SPEED control S2. With S2 in the FAST position, the high signal at U7-9 is

NAND-ed with the $\overline{\text{RECORD}}$ signal to drive U7-8 low. This low signal drives U8-3 high, which disables the slow clock pulses at U8-3. Similarly, when the U7-3 signal is low (inverted by U7B), it enables the fast clock through U7D.

When the MEMORY STEP switch is depressed, the high signal generated at U10-6 clocks U24. The high signal at U24-5 starts oscillator U1C-U1D. Since U6 has been reset, the output of U2E is high, which creates the other oscillator signal at U1-10. Each clock-pulse output by frequency-divider U5 creates an external clock pulse at U10-11. A sequence is generated similar to that in the SAMPLE mode, except for the gating at U4D. The SAMPLE signal is high, which allows the reset pulse from U1A to pass through to Q2. Q2, in turn, resets the COUNTER GATE in the data acquisition module. The low SAMPLE signal places Q1 in an on condition, preventing the writing of data into memory.

MANUAL operation with the SLOW scan speed is identical to that with the FAST scan speed, except the logic controls the SLOW clock chain through U8A and U8B while disabling U7D.

The data are converted and displayed when the STROBE signal is high and the time generator is disabled.

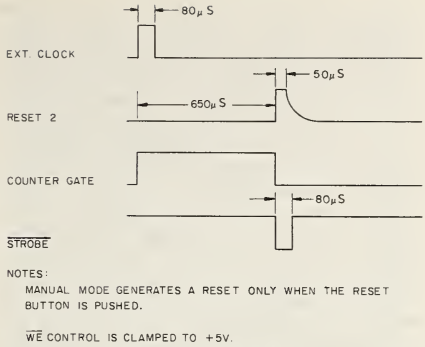


FIGURE 25.—Timing diagram for data retrieval and recorder unit in MANUAL mode.

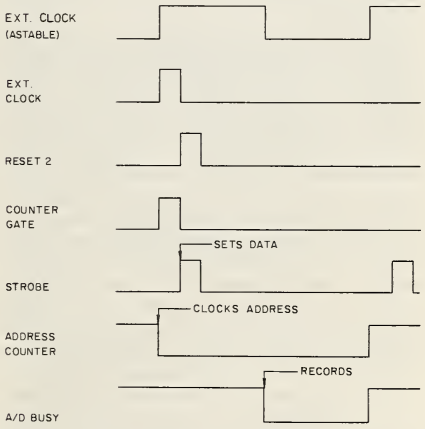


FIGURE 26.—Timing diagram for data retrieval and recorder unit in RECORD mode.

RECORD MODE

The RECORD mode of operation is somewhat more complex than the other two modes because it involves two additional subassemblies, the tape recorder interface and the recorder, along with all of the other subassemblies. A timing diagram for the unit in the RECORD mode is shown in figure 26.

When MODE switch S6 is in the $\overline{\text{RECORD}}$ position, the $\overline{\text{RECORD}}$ signal at U13-11 is low, which disables the MEMORY STEP function by driving U9-6 high. This high signal disables the STEP flip-flop at U9-12 and enables the clock-chain signal going to the pulse generator (C4a, R7, and U10D). The $\overline{\text{RECORD}}$ signal also drives U7-10 low, which disables the SCAN SPEED control, and selects the 1-s clock.

The RECORD signal at U15-10 enables END OF RECORD (EOR) gate U13B and recorder A/D BUSY gate U20A. The high RECORD signals at U14-4 and U16-13 reset DATA SELECT flip-flop U14.

Since no clock pulses have been supplied to U6, the RECORD ENABLE signal (output of U2E) is high, which causes a high at U13-4. The high signal at U13-4 is NAND-ed with the RECORD signal to cause a high at U14-13. This high signal enables RECORDER ENABLE flip-flop U14B. The high signal at U4-10 from U14-8 is NAND-

ed with the high SYNC pulse to provide a RESET 1 pulse to the data acquisition module, which resets the address register. The SYNC pulse also resets the DATA SELECT flip-flop, which allows U22 and U23 to be loaded with the data (time) contained in thumb-wheel switches S10–S13.

When MEMORY STEP switch S4 is depressed and released, a series of clock pulses is simultaneously transmitted to the recorder as A/D BUSY pulses and to the data acquisition module as EXTERNAL CLOCK pulses. The reset pulse generator at U1–3 holds the memory address register at address zero while the DATA SELECT low signal allows data to be transferred from the recorder data bus, which results in the recording of zeroes for data. The $\overline{\text{DATA SELECT}}$ signal at U11–13 prevents the time generator from being clocked by the A/D BUSY or WORD COUNTER signals. Recording of one file of zeroes (see appendix A) is a good way to synchronize the recorder and thereby avoid the loss of valid data.

When the recorder completes the recording of eight data words (still all zeroes at this time), a WORD COUNTER pulse is received from the recorder via U12A, which clocks the DATA SELECT flip-flop and also generates an EOF pulse. This pulse is written on the magnetic tape to indicate the end of a line of data. The recorder acknowledges the EOF and returns an EOF to the tape recorder interface. The rising edge of the EOF signal initiates a 0.15-s delay, generated by U19A, C9, CR2, R23, and U19B, to allow the recorder time to record a 3-bit gap (a feature Datel has installed in the recorder to increase the reliability of recorded data). A START 2 signal is then sent to the recorder by U20C, which puts the recorder in the serial-data mode. This procedure allows the data (time of day) that was previously loaded into U22 and U23 to be shifted out to the recorder via shift registers U17 and U18. After 16 SHIFT CLOCK pulses have been returned from the recorder (about 0.15 s), START 2 goes to a low signal and indirectly generates another EOF. (Appendix A shows the resulting format of parallel data (temperature data + ID number) and serial data (military time).) The EOF returned from the recorder will not cause a START 2 signal, since the A/D BUSY signal is high and blocks the generation of another EOF at U20–10.

DATA SELECT is reenabled which, in turn, disables U4A and blocks the reset pulse from the data acquisition module. The next clock pulse advances the memory address register to location 001. The binary-to-BCD converter decodes the number (temperature data) stored in memory location 001, and the DATA SELECT signal places the data on the recorder data bus. The falling edge of the external clock pulse generates an A/D BUSY signal and allows the data to be transferred (recorded).

If SAMPLE INTERVAL switch S7 is set for 8 words per hour, A/D BUSY is passed through U11A, U11B, U12B, and U11D to clock U22 once after each 8-word interval (the data in memory addresses 001–008). If S7 is set for 1 word per hour, U22 is clocked through U11C, U11B, U12D, and U11D, which causes U22 to be incremented 1 h for each data word. The tape recorder interface then generates an EOF signal and passes the serial data out, etc., which is repeated until all 256 or 512 memory locations have been recorded. The signal at U2–10 then goes low, resetting U14B and disabling the timing chain.

CALIBRATION OF DATA ACQUISITION MODULES

Each module has a slightly unique calibration curve for temperature-vs.-oscillator frequency. The first source of variance results from inconsistency among components of the oscillator circuits, primarily the resistors and capacitor C6. The second, and more pronounced, variance is due to the resistance-vs.-temperature characteristics of the thermistor. We use interchangeable precision thermistors and thus avoid the second source of variance.

If ordinary tolerance (5% to 20%) thermistors are used, each unit must be calibrated by immersing the thermistor in a controlled-temperature water bath and observing the frequency at increments of about 0.5° C over the range of temperature of interest. For animal-body temperature, a range of 35° to 45° C is adequate. If precision thermistors are used, a precision decade resistor can be used in lieu of a thermistor, since the resistance for various temperatures will be known. The resistance is then changed in increments corresponding to temperature increments of about 0.5° C, and again the frequency is observed and recorded. This method speeds up the time required for calibration because one does

not have to wait for the water-bath temperature to stabilize after each change in temperature.

Since a computer is used to process and analyze the data, we derive a regression equation of temperature vs. frequency for each data acquisition module. A second- or third-order polynomial equation provides a good fit. For a range in temperature of 10° C, the resolution is 10° C÷256 (limited by 8 bits)=0.039° C/Hz.

We have determined that drift over time is negligible providing the battery is changed within 1 mo after being placed in service and that ambient temperature has negligible effect on the frequency of the oscillator.

CONNECTER CHARTS AND PARTS LISTS

The connecter charts are given in appendices B–H. These data are provided to assist the reader in determining the interconnections between various subassemblies.

The major components required for construction of a data acquisition module are listed in appendix I. The major components required for construction of the logic board of the data retrieval and recorder unit are listed in appendix J. The parts for the remainder of the data retrieval and recorder unit, including the displays, power supply, connecter board, binary-to-BCD connecter, and front panel (including case), are listed in appendix K. The layout for the p.c. boards is not shown, since one desiring to construct a unit would probably use their own design and layout.

DISCUSSION OF PERFORMANCE

The data acquisition system has performed well in limited tests, both in the field and in the laboratory. Some of the data acquisition modules have failed to store the correct number of readings during field use. We believe this failure may have been the results of momentary power loss caused by extremely hard blows to the modules once they were attached to a halter on 400- to 500-lb calves.

We have also determined that the rate of transfer of data from the memory in the data acquisition module to the magnetic tape in the data retrieval and recorder unit is somewhat slow. This slowness of data transfer is a disadvantage when monitoring the temperature of animals, since they must be held in a squeeze chute for approximately 10 min, but it would present no problems in many other applications where the data could be transferred leisurely, probably at the end of the monitoring period.

The system exceeds the original design in all respects and would be excellent for monitoring temperature and other measurements during domestic or foreign shipments. This system can be constructed by anyone having a rather extensive background in digital electronic circuits. Rockwall Communications Center, Arlington, Tex., constructed the final units for us and has the capabilities to reproduce the system for the user who wishes to purchase rather than construct the system.

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APPENDIX A.—TYPICAL DATA IN A FORMAT SUITABLE FOR COMPUTER PROCESSING

```
ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4
1Ø44                                                          Time (military)
ØØØ 4   ØØØ 4   ØØØ 4   Ø88 4   Ø88 4   Ø84 4   Ø84 4   Ø83 4
1844
Ø77 4   Ø77 4   Ø76 4   Ø74 4   Ø72 4   Ø7Ø 4   Ø69 4   Ø77 4
Ø244
Ø73 4   Ø72 4   Ø72 4   Ø67 4   Ø64 4   Ø56 4   Ø66 4   Ø85 4
1Ø44                                                          Data, oscillator
Ø8Ø 4   Ø78 4   Ø77 4   Ø81 4   Ø83 4   Ø86 4   Ø87 4   Ø85 4   frequency corre-
1844                                                          sponding to a
Ø85 4   Ø86 4   Ø9Ø 4   Ø81 4   Ø85 4   Ø8Ø 4   Ø81 4   Ø84 4   temperature
Ø244
Ø8Ø 4   Ø77 4   Ø76 4   Ø79 4   Ø87 4   Ø75 4   Ø67 4   Ø74 4
1Ø44
Ø88 4   Ø9Ø 4   Ø9Ø 4   Ø92 4   Ø98 4   1Ø3 4   112 4   118 4
1844
118 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4   ØØØ 4
                                                              File of zeroes to
Ø239                                                          insure no real data
ØØØ B   ØØØ B   ØØØ B   ØØØ B   ØØØ B   ØØØ B   ØØØ B   ØØØ B   are lost because of
1Ø39                                                          lack of synchro-
ØØØ B   ØØØ B   ØØØ B   Ø94 B   Ø92 B   Ø92 B   Ø96 B   Ø93 B   nization between
1839                                                          recorder and re-
Ø89 B   Ø84 B   Ø85 B   Ø8Ø B   Ø78 B   Ø76 B   Ø76 B   Ø71 B   corder interface
Ø239
Ø68 B   Ø64 B   Ø65 B   Ø6Ø B   Ø64 B   Ø75 B   Ø73 B   Ø71 B
1Ø39
Ø69 B   Ø68 B   Ø65 B   Ø64 B   Ø72 B   Ø69 B   Ø67 B   Ø71 B
1839
Ø68 B   Ø67 B   Ø7Ø B   Ø67 B   Ø64 B   Ø63 B   Ø62 B   Ø61 B
Ø239                                                          Module ID number
Ø66 B   Ø62 B   Ø59 B   Ø57 B   Ø57 B   Ø62 B   Ø6Ø B   Ø58 B
1Ø39
Ø6Ø B   Ø62 B   Ø62 B   Ø64 B   Ø63 B   Ø65 B   Ø67 B   Ø68 B
1839
Ø68 B   Ø73 B   Ø68 B   Ø65 B   Ø64 B   Ø61 B   Ø64 B   Ø59 B
Ø239
Ø6Ø B   Ø63 B   Ø6Ø B   Ø62 B   Ø65 B   Ø88 B   Ø91 B   Ø91 B
1Ø39
Ø89 B   Ø92 B   Ø96 B   1Ø2 B   1Ø7 B   115 B   112 B   ØØØ B
```

APPENDIX B.—FRONT PANEL CONNECTIONS

1.	Power on	Voltage regulators
2.	Charge	Charger connecter
3.	Power common	Battery+
4.	Display on	Both display boards
5.	Display common	Ground
6.	Load forward NC (S8)	Logic P1-25
7.	Load forward NO (S8)	Logic P1-13
8.	Load forward common (S8)	Ground
9.	Manual mode (S6)	Logic J2-22
10.	Sample mode (S6)	Logic J2-21
11.	Mode common (S6)	Ground
12.	Step NO (S4)	Logic J2-19
13.	Step NC (S4)	Logic J2-18
14.	Step common (S4)	Ground
15.	Reset NO (S5)	Logic J2-7
16.	Reset NC (S5)	No connection
17.	Reset common	Ground
18.	256 (S1)	Logic J2-8
19.	512 (S1)	Logic P1-19
20.	256/512 (S1)	Logic J2-20
21.	Interval common (S7)	Ground
22.	8/h	Logic J2-15
23.	1/h	Logic J2-16
24.	Step select common (S4)	Ground
25.	Scan (S3)	Logic J2-17
26.	Single (S3)	No connection
27.	Scan speed common (S2)	Ground
28.	Fast	Logic J2-24
29.	Slow	Logic J2-23
30.	ID common	+5 V
31.	A_{ID}	Recorder
32.	E_{ID}	Recorder
33.	C_{ID}	Recorder
34.	D_{ID}	Recorder
35.	H_{10} common	+12 V
36.	H_1 common	+12 V
37.	M_{10} common	+12 V
38.	M_1 common	+12 V
39.	A_{H1}	Logic J2-10
40.	B_{H1}	Logic J2-13
41.	C_{H1}	Logic J2-9
42.	D_{H1}	Logic J2-12
43.	A_{H10}	Logic J2-4
44.	B_{H10}	Logic J2-6
45.	A_{M1}	Logic P1-5
46.	B_{M1}	Logic P1-4
47.	C_{M1}	Logic P1-3
48.	D_{M1}	Logic P1-11
49.	A_{M10}	Logic P1-9
50.	B_{M10}	Logic P1-8
51.	C_{M10}	Logic P1-7
52.	D_{M10}	Logic P1-6

APPENDIX C.— DATA DISPLAY CONNECTIONS

Terminal	Signal	
1	A_1	Buffered to 5-V TTL
2	B_1	
3	C_1	
4	D_1	
5	A_{10}	
6	B_{10}	
7	C_{10}	
8	D_{10}	
9	A_{100}	
10	B_{100}	
11	+5 V	
12	Ground	
13	Display	

APPENDIX D.— ADDRESS DISPLAY CONNECTIONS

1. Clock
2. Reset
3. +5 V
4. Display
5. Ground

APPENDIX E.—PIN ASSIGNMENTS FOR CONNECTERS P1 AND J2

Connecter P1	
Pin	Function
1	Reset 1
2	Ext. clock
3	C_{M1}
4	B_{M1}
5	A_{M1}
6	D_{M10}
7	C_{M10}
8	B_{M10}
9	A_{M10}
10	Shift clock (recorder)
11	D_{M1}
12	Serial data out (recorder)
13	Load forward NO (recorder)
14	Ground
15	Reset 2
16	WE out
17	+5 V
18	+12 V
19	Memory size select 512 (S1)
20	Data select (recorder)
21	A/D BUSY (recorder)
22	START TWO (recorder)
23	Ext. EOF (recorder)
24	Load forward out (recorder) (S8)
25	Load forward NC (recorder) (S8)

Connecter J2	
Pin	Function
1	No connection
2	No connection
3	D_{H10}
4	A_{H10}
5	C_{H10}
6	B_{H10}
7	Reset SW (SJ)
8	Memory size select 256(S1)
9	C_{H1}
10	A_{H1}
11	Word counter in (recorder)
12	D_{H1}
13	B_{H1}
14	No connection
15	Sample interval select 8/h (S7)
16	Sample interval select 1/h (S7)
17	Scan (33)
18	Memory step NC (S4)
19	Memory step NO (S4)
20	Memory size select commons (S1)
21	Sample mode (S6)
22	Manual mode (S6)
23	Scan rate slow (S2)
24	Scan rate fast (S2)
25	EOF in (recorder)

APPENDIX F.—PIN ASSIGNMENTS FOR CONNECTER P3, HEX-TO-BCD CONVERTER

Pin	Function
1	Counter gate input
2	Counter gate output
3	B_{100}
4	A_{100}
5	Data select
6	B_7
7	B_6
8	B_5
9	B_4
10	B_3
11	B_2
12	B_1
13	B_0
14	Ground
15	+5 V
16	+12 V
17	C_{10}
18	D_{10}
19	B_{10}
20	A_{10}
21	A_1
22	B_1
23	C_1
24	D_1
25	Spare

APPENDIX G.—PIN ASSIGNMENTS FOR CONNECTER J5, DATA ACQUISITION MODULE

Pin	Function	Color
1	B_4	red
2	B_7	yellow
3	B_6	blue
4	B_5	grey
5	B_0	black
6	B_3	red
7	B_2	yellow
8	B_1	blue
9	Data	green
10	+5 V	orange
11	Counter gate	brown
12	Reset	white
13	$\overline{WE}$	purple
14	Ground	green
15	Spare	orange
16	Clock	brown

APPENDIX H.—PIN ASSIGNMENTS FOR CONNECTER J6, DATEL RECORDER

Pin	Function	Pin	Function
1	Ground	A	Not used
2	Ground	B	Not used
3	B_{100}	C	Not used
4	A_{100}	D	Not used
5	D_{10}	E	Not used
6	C_{10}	F	Not used
7	B_{10}	H	Not used
8	A_{10}	J	Word counter out
9	D_1	K	Not used
10	C_1	L	Load forward
11	B_1	M	Ground
12	A_1	N	Not used
13	Not used	P	Write ext. EOF
14	Ground	R	Not used
15	+12 V d.c.	S	Not used
16	Not used	T	Not used
17	Not used	U	Not used
18	EOF Out	V	Not used
19	A_{ID}	W	A/D BUSY
20	B_{ID}	X	START TWO
21	C_{ID}	Y	Data select
22	D_{ID}	Z	Serial data in

APPENDIX I.—
REFERENCE DESCRIPTIONS AND COMPONENTS FOR DATA ACQUISITION MODULE

Integrated circuits:
- U1—14-stage binary counter (National 4060 or equivalent)
- U2, U4, U8—12-stage binary counter (National 4040 or equivalent)
- U3—Dual D flip-flop (National 4013 or equivalent)
- U5—Triple op-amp (Siliconix L-144 or equivalent)
- U6, U7—256×4 CMOS memory (Harris 6551 or equivalent)
- U9—Voltage reference diode (National LM103-5.1 or equivalent)

Transistor & diodes:
- Q1 (Motorola 2N930 or equivalent)
- CR2, CR3 (General Electric 1N34 or equivalent)

Resistors, 1/10 W, 5% tolerance, carbon film:
- R1—1 MΩ
- R4, R18—10 kΩ
- R2—10 MΩ
- R3, R5-R11, R13-R15, R19, R20—100 kΩ
- R12—33 kΩ
- R16—220 kΩ
- R17—470 kΩ
- R21—27 kΩ

Capacitors, monolithic, ceramic, 50 working volts direct current (WVDC), 10% tolerance:
- C1—10 pF
- C2—5 pF
- C3-C5, C7—0.001μF
- C6—0.033μF
- C8, tantalum—4.7μF

Miscellaneous:
- S1a, S1b, S1c, S1d—Switch, 4-gang, DIP
- Y1—Crystal, 18.641 kHz
- J5—Socket, 16-pin, DIP, with 2-ft ribbon cable
- B1—Battery, 7.5-V (Mallory TR 175 or equivalent)
- R22—Thermistor, 100 kΩ at 25° C
- No designation:
  - P.C. boards (4 each)
  - Case, 3 mm-thick machined aluminum, 45 mm wide, 90 mm long, and 20 mm high

APPENDIX J.—REFERENCE DESCRIPTIONS AND COMPONENTS FOR LOGIC BOARD OF DATA RETRIEVAL AND RECORDER UNIT

Integrated circuits:
- U1, U4, U7-U11, U13, U20, U21—Quad 2-input NAND gate (National 74C00 or equivalent)
- U2, U12, U15, U19—HEX inverter (National 74C04 or equivalent)
- U3—HEX buffer, noninverting; CMOS to TTL (National 74C902 or equivalent)
- U5—7-Stage binary counter (National 4024 or equivalent)
- U6—14-Stage binary counter (National 4040 or equivalent)
- U14, U24—Dual D flip-flop (National 74C74 or equivalent)
- U16—Triple 3-input NAND gate (National 74C10 or equivalent)
- U17, U18—8-Bit, parallel in/serial out shift register (National 74C165 or equivalent)
- U22, U23—Presettable decade up/down counter (National 74C192 or equivalent)

Transistors & diodes:
- Q1, Q2 (Motorola 2N2907 or equivalent)
- Q3 (Motorola 2N2222 or equivalent)
- CR1, CR2 (General Electric 1N4148 or equivalent)

Resistors, 1/4 W, 5% tolerance, carbon film:
- R1-R14, R16-R22, R24, R25—100 kΩ
- R23—1 MΩ
- R15—10 kΩ

Capacitors, monolithic, ceramic, 50 WVDC, 10% tolerance:
- C1, C3, C10, C11—0.001 μ F
- C4, C6-C8—0.01 μ F
- C2—0.1 μ F
- C9—0.15 μ F
- C5—1.0 μ F

Miscellaneous:
- S1-S3, S6, S7—Switch, SP, on-on
- S4, S5, S8—Switch, SPDT, on-on
- S14—Switch, DP, on-on
- S10-S13—Switch, BCD thumb-wheel
- S15—Switch, HEX thumb-wheel
- No designation:
  - P.C. board
  - P1—Connecter, plug, 25-pin D-subminiature
  - J2—Connecter, jack, 25-pin D-subminiature

APPENDIX K.—REFERENCE DESCRIPTIONS AND COMPONENTS FOR BINARY-TO-BCD CONVERTER, DISPLAYS, CONNECTER BOARD, POWER SUPPLY, AND FRONT PANEL

Integrated circuits and displays:
- U101, U102—HEX buffer, noninverting; CMOS to TTL (National 74C902 or equivalent)
- U103–U105—Binary-to-BCD converter (TTL) (National 74185 or equivalent)
- U106–U108—Quad 2-input NAND gate (National 74C00 or equivalent)
- U201—4-Decade counter, multiplexed output (National 74C925 or equivalent)
- U202–U204, U302, U304, U306—7-Segment display (Hewlett Packard 7740 or equivalent)
- U301, U303, U305—BCD to 7-segment decoder (National 74C48 or equivalent)
- U401—Voltage regulator (National LM304-5 or equivalent)
- U402—Voltage regulator (National LM304-12 or equivalent)
- U403, U404—HEX inverter with open collector (Texas Instruments 7205 or equivalent)

Transistors & diodes:
- Q201–Q203 (Motorola 2N2222 or equivalent)
- CR401 (Motorola 1N4001 or equivalent)

Resistors, 1/4 W, 5% tolerance, carbon film:
- R101–R110, R401–R431—100 kΩ
- R201–R207—200Ω
- R301–R303—220Ω

Capacitors, electrolytic, 24 WVDC, tolerance: −10% to +75%
- C401, C403, C405—330 μF
- C402, C404—22 μF

Miscellaneous:
- J1, J3—Connecter, jack, 25-pin D-subminiature
- P2, P5—Connecter, plug, 25-pin D-subminiature
- J6—Connecter, jack, 44-pin, p.c. card edge
- B401—Battery, 16-V nicad
- F401—Fuse, AGC 5-A
- S401—Switch, DPDT, on-off-on, 6-A
- No designation:
  - P.C. board (2 each)
  - Case, fiberglass, about 230 mm wide, 380 mm long, and 205 mm high (Ladies' train case or equivalent)
  - Front panel, shop-constructed (see fig. 8)

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